

Electrical Characteristics of Oxide Thin-Film Transistors for Stretchable Displays Using a Triple-Layer Gate Dielectric

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ABSTRACT: There is an increasing demand for freeform stretchable display technologies capable of overcoming spatial limitations in next-generation platforms such as augmented reality (AR) and virtual reality (VR). To realize such stretchable displays, all constituent materials—including semiconductors, electrodes, insulators, and substrates—must exhibit sufficient mechanical elasticity. To date, stretchable gate insulators have primarily relied on organic polymers such as poly(4-vinylphenol-co-methyl methacrylate) (PVP-co-PMMA). However, their practical application is significantly limited by poor electrical properties, including low dielectric constant and instability. In this work, we propose a novel gate insulator structure that minimizes the use of solution-based processes, which often suffer from poor uniformity and may damage underlying layers during fabrication. The proposed structure integrates the advantages of both organic and inorganic materials by employing a hybrid configuration. Specifically, high-k HfO₂ thin films are deposited on both the top and bottom of an organic layer composed of PVP-co-PMMA, poly(melamine-co-formaldehyde) (PMF) as a crosslinking agent, and propylene glycol monomethyl ether acetate (PGMEA) as a solvent. This inorganic–organic–inorganic structure effectively compensates for the inherent electrical limitations of organic materials. As a result, the fabricated thin-film transistors (TFTs) exhibit improved electrical performance and reliability compared to devices employing a single organic gate insulator.

KEYWORDS: Stretchable displays, Gate dielectric, Oxide, Transistors, PVP-co-PMMA, HfO₂

1 Introduction

The development of freeform displays, including flexible and stretchable displays, is becoming increasingly important for next-generation technologies such as mobile devices, augmented reality (AR), virtual reality (VR), and bio-integrated systems [1–3]. To realize such systems, all components of the display—including semiconductors, electrodes, insulators, and substrates—must exhibit mechanical flexibility and stretchability. Organic materials such as poly(4-vinylphenol-co-methyl methacrylate) (PVP-co-PMMA) have been widely used as flexible gate insulators due to

their mechanical compliance [4–8]. However, their application is limited by poor electrical properties, including low dielectric constant and instability. Moreover, while flexible substrates (e.g., PDMS laminated with polyimide (PI)) have been explored, prior studies primarily focus on substrate design without proposing a complete device architecture suitable for stretchable displays.

Additionally, thin-film transistor (TFT) devices used as backplanes must be fabricated on flexible substrates in order to achieve flexible and stretchable displays. There are few reports of previous studies in which the gate insulator layer of TFT devices was fabricated using a solution process, despite the fact that a

considerable number of studies have previously reported on the electrical characteristics of TFT devices using oxide semiconductors as the channel layer based on solution processes [9,10]. In this study, we propose a hybrid inorganic–organic–inorganic (IOI) gate insulator structure that combines the electrical advantages of inorganic materials with the mechanical flexibility of organic materials. By minimizing reliance on solution-based processes—which often suffer from poor reproducibility and potential damage to underlying layers — we demonstrate improved electrical performance and reliability in oxide thin-film transistors (TFTs).

2 Device Design and Fabrication

To realize stretchable oxide TFTs, a composite elastic substrate was fabricated by stacking a polyimide (PI) layer onto a polydimethylsiloxane (PDMS) layer, as illustrated in Fig. 1. The PI layer provides mechanical rigidity, while PDMS contributes high elasticity. This combination enables both structural stability and stretchability. The fabrication process begins with a sacrificial substrate, onto which the PI layer is deposited. After removing the

sacrificial substrate, PDMS is formed beneath the PI layer. A buffer layer is subsequently introduced on top of the PI surface to protect the substrate and ensure stable device fabrication. A 100 nm thick HfO_2 layer was deposited using atomic layer deposition (ALD) at 150°C . Source and drain electrodes were then formed by sputtering 200-nm-thick molybdenum (Mo) layers. Subsequently, a 20-nm-thick indium-gallium-zinc oxide (IGZO) semiconductor layer was deposited via plasma-enhanced ALD (PEALD).

3 Gate Insulator Engineering

The gate insulator in this study was a triple-layer structure composed of an organic layer (PVP-co-PMMA (50 nm)), a top inorganic layer (HfO_2 , 10 nm), and a bottom inorganic layer (HfO_2 , 15 nm). We'll go into more depth on the particular process for manufacturing the gate insulating layer. To create a lower inorganic layer, HfO_2 is first deposited using ALD process on the whole top surface of the semiconductor layer, source, and drain metal layers. To avoid harming the IGZO semiconductor layer created below, the deposition temperature in this method is

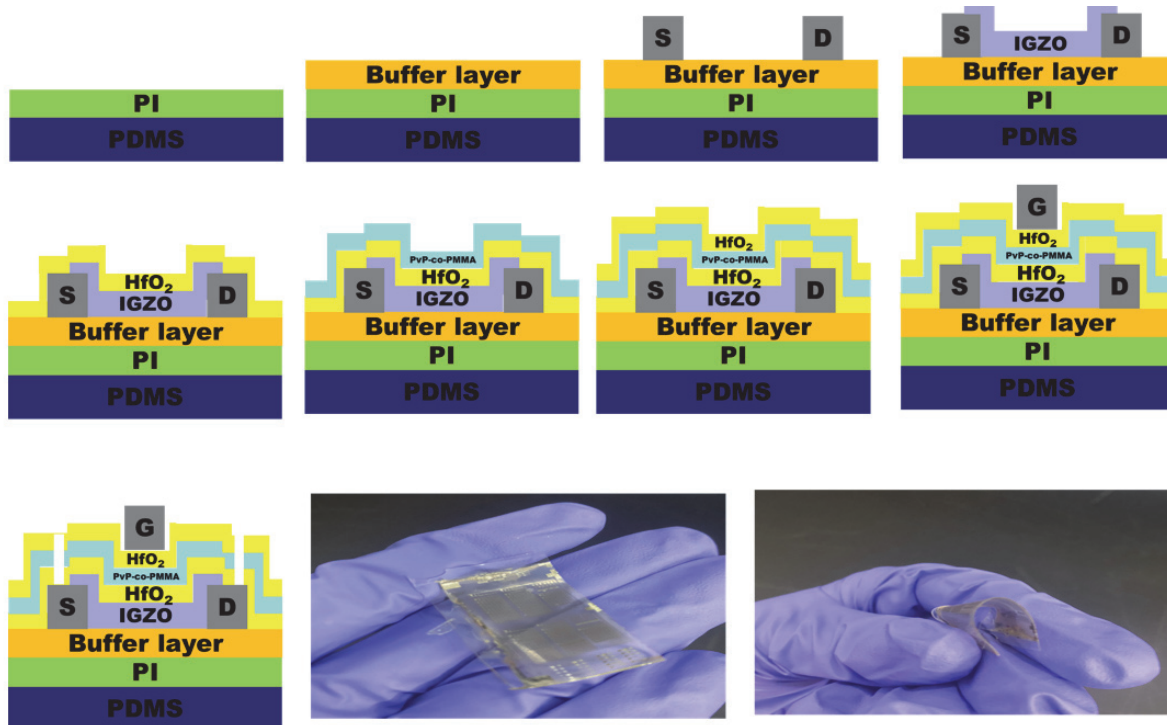


Fig. 1. Cross-sectional schematic of a stretchable thin-film semiconductor device during fabrication

adjusted to 150°C. The thickness of the lower inorganic layer is formed to a thickness of 25 nm.

The bottom inorganic layer is then covered with an organic layer by spin-coating and curing procedures. Below is a detailed description of the particular process used to generate the organic layer. PvP-co-PMMA (4 weight percent), PGMEA (propylene glycol monomethyl ether acetate) 5 mL, and PMF (poly-methoxy flavones) (4 weight percent) are first combined. At 75°C and atmospheric pressure, the mixture is agitated for 12 hours. The organic layer, which is made up of PvP-co-PMMA, is made better by this stirring procedure. In particular, raising the stirring temperature eliminates moisture, which lowers viscosity. The cross-linking reaction becomes more uniform when the viscosity is reduced. When used as a gate insulating layer, increasing the cross-linking reaction's homogeneity successfully stops leakage current. Propylene glycol and methanol are produced during the hydrolysis of PGMEA, which is utilized as a solvent and includes ester linkages.

Substances with OH groups may be formed as a result of this mechanism. The gate insulating film's roughness may be increased by water or OH groups. MgSO₄ was added to reduce the effects of water and OH groups, preventing an increase in the organic layer's roughness. In this case, 2 weight percent of MgSO₄ 4.78 g can be added to the 98-weight percent mixture of the previously mentioned blend (PvP-co-PMMA, PGMEA (propylene glycol monomethyl ether acetate), and PMF (poly-methoxy flavones). Since MgSO₄'s only function is to react with water molecules to precipitate water, the precise amount of MgSO₄ supplied is not important; consequently, MgSO₄ can be combined with 1–99 weight percent of the mixture. It was confirmed that the roughness was 0.170 nm with MgSO₄ and 0.203 nm without it. The mixture was then deposited onto the upper surface of the bottom inorganic layer after being filtered to remove contaminants. For this coating procedure, spin coating is an option. The solution was pre-filtered using a 0.2 μm syringe filter in preparation for the spin-coating procedure. The spin-coating process was subsequently carried out for about 30 seconds at speeds of 500, 1,000, and 1,500 RPM, according to the order, after the substrate was set on the spin coater and the solution was dispensed. The organic layer was then created by pre-baking for ten minutes at 100°C, UV treatment for ten minutes, and annealing for three hours at 150°C.

The homogeneity of the cross-linking process is improved by increasing the stirring temperature to 75°C, which lowers the viscosity of the reactants (PMF: PvP-co-PMMA: PGMEA). As a result, leakage current in the gate insulating layer can be effectively controlled. Ester bonds are present in PGMEA, a solvent.

Propylene glycol and methanol are produced when PGMEA hydrolyzes, and it's possible that compounds with OH groups will also be created. In this experiment, MgSO₄ was added to eliminate the H₂O and OH groups that can increase the roughness of the gate insulating film, and it was confirmed that they were successfully removed as shown in Table 1. Improvement of PvP-co-PMMA film quality according to stirring temperature and moisture removal were verified.

Graphs of the Fourier transform infrared (FT-IR) spectroscopy results for a number of experimental cases are displayed in Fig. 2. The results for stirring at room temperature without adding MgSO₄ are shown in Fig. 2(a); the results for stirring at room temperature with MgSO₄ added are shown in Fig. 2(b); the results for stirring at 75°C without adding MgSO₄ are shown in Fig. 2(c); and the results for stirring at 75°C with MgSO₄ added are shown in Fig. 2(d). The current invention's process conditions are shown in Fig. 2(d). It is proven that when MgSO₄ was added at room

Table 1. Changes in atomic force microscope (AFM) roughness of thin films due to temperature and moisture removal

	Rq (nm)	Ra (nm)
Stirring at RT	0.387	0.35
Stirring at 75°C	0.278	0.221
Stirring at RT (added MgSO ₄)	0.291	0.286
Stirring at 75°C (added MgSO ₄)	0.203	0.17

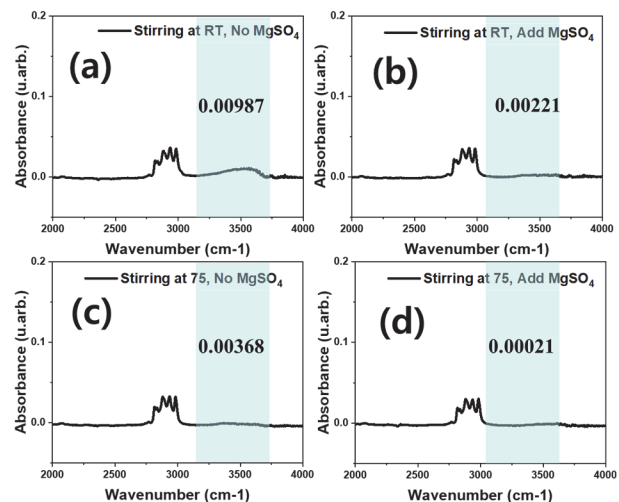


Fig. 2. FT-IR characteristics of (a) stirring at room temperature (RT) without MgSO₄, (b) stirring at RT with MgSO₄, (c) stirring at 75°C without MgSO₄, and (d) stirring at 75°C with MgSO₄

temperature (Fig. 2(b)), the OH peak (3100–3700) was reduced to about one-fourth of what was seen when MgSO_4 was not introduced at room temperature (Fig. 2(a)). Additionally, when MgSO_4 is not supplied at 75°C, the peak is reduced by about one-third (Fig. 2(c)), but when MgSO_4 is introduced at 75°C, it is reduced by a factor of 47. Both the reactant concentration and the thin film's roughness are impacted by this variation.

The organic layer was followed by the formation of an upper inorganic layer. The higher inorganic layer shared the same thickness and creation process as the lower inorganic layer. The gate insulator used in this work was a layered structure made up of an organic layer, an upper inorganic layer, and a lower inorganic layer. A single inorganic layer is the most effective way to obtain the electrical characteristics of semiconductor devices, according to experimental confirmation; nevertheless, this layer is insufficient to meet the tensile strength requirements of flexible devices. In order to guarantee tensile strength, a bilayer structure with an organic layer at the bottom and an inorganic layer at the top may be taken into consideration. However, when the organic material came into contact with the semiconductor layer, the device's electrical properties declined. A bottom inorganic layer, an organic layer, and a top inorganic layer make up the triple-layer gate insulator construction we presented in this study. We verified that this structure not only guarantees tensile strength but also keeps the organic layer away from the semiconductor layer, preventing the electrical properties of the device from deteriorating.

Using a traditional single PI layer makes it challenging to achieve a stretchable display, which needs strong elasticity in both the vertical and horizontal planes. A highly elastic PDMS layer was put underneath the traditional PI substrate to solve this. Additionally, an organic PVP-co-PMMA insulating film was coated in between an inorganic HfO_2 insulating film that was produced on both the top and bottom surfaces using atomic layer deposition (ALD) at a low process temperature of 150°C or less. As seen in Fig. 3 below, increasing the ALD deposition temperature to 250°C causes the PI film to wrinkle, which is why we restricted the ALD deposition temperature for the HfO_2 thin-films to 150°C or below. This resulted in the development of a hybrid organic-inorganic insulating film structure that was stretchable at low process temperatures. The gate insulating film for TFT devices was subsequently used. Following the formation of the gate insulator, a 200-nm-thick layer of molybdenum metal was sputter-deposited on top of it and then patterned to create the gate metal layer.

The electrical characteristics of a single-layer HfO_2 gate insulator,

a PVP-co-PMMA and HfO_2 double-layer gate insulator, and the triple-layer gate insulator of the oxide TFTs compared in Fig. 4. While TFT devices with a single HfO_2 gate insulator exhibit the best electrical characteristics (such as subthreshold swing (S.S.) and $I_{\text{ON/OFF}}$), they do not meet the tensile strength requirements for stretchable TFTs. In the case of a PVP-co-PMMA and HfO_2 double-gate insulator, it has been confirmed that the organic material comes into contact with the oxide semiconductor layer, degrading the semiconductor characteristics. Accordingly, it has been confirmed that depositing inorganic materials such as HfO_2 above and below the organic material improves the device's electrical characteristics while also ensuring tensile strength.

The electrical reliability of oxide TFT devices with three different gate dielectric structures has been evaluated in addition to their electric characteristics. The transfer characteristics ($I_{\text{DS}}-V_{\text{GS}}$) of oxide TFTs with different three gate insulator structures under a positive gate bias (10 V) are shown in Fig. 5, while those under a negative gate bias (-10 V) are presented in Fig. 6. The oxide semiconductor layer in contact with the organic layer was responsible for the observable deterioration and conductive behavior in the bilayer structure, while the triple-layer structure showed a positive shift phenomenon instead of the usual negative bias stability behavior. Consequently, it was verified that the HfO_2 -PVP-co-PMMA- HfO_2 triple-layer structure suggested in this work had advantageous transfer characteristics. This implies that the organic layer treatment minimizes performance degradation by preventing leakage current production.

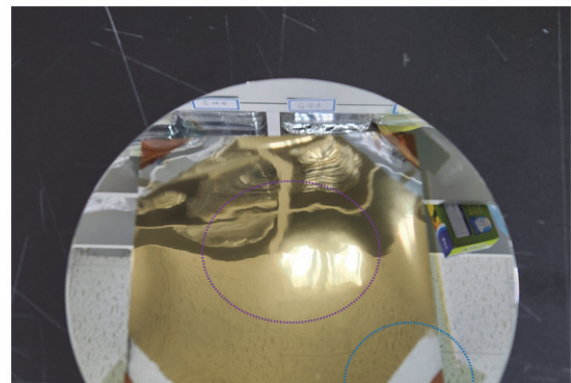


Fig. 3. A PI layer that has been bonded to the top of a 6-inch wafer warps when the ALD process is performed at a substrate temperature of 250°C (Gate insulators: HfO_2 thin-films)

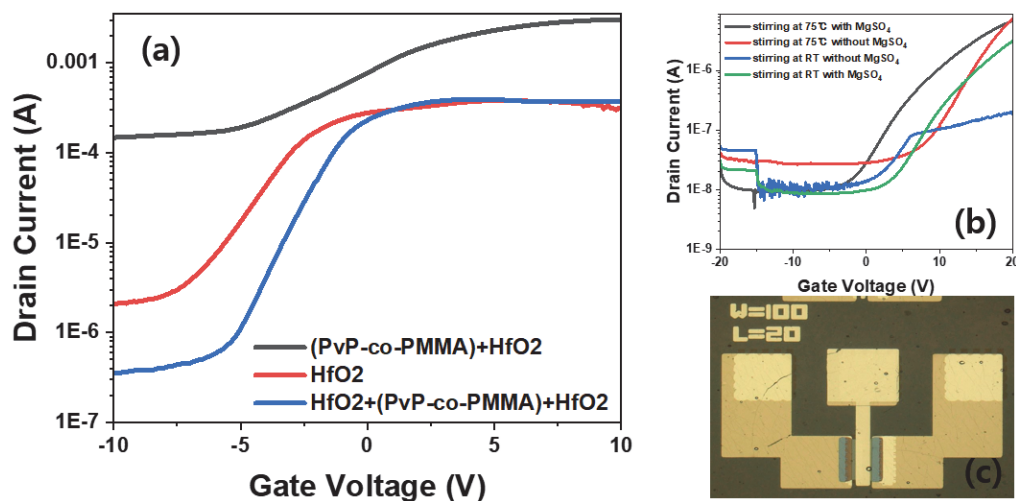


Fig. 4. Transfer characteristics of (a) oxide TFTs with single-, double-, and triple-layer gate insulators, (b) different stirring conditions on silicon wafers; and (c) optical microscope image of stretchable oxide TFTs. The electrical properties of a single-layer HfO_2 gate insulator, a double-layer gate insulator made of PvP-co-PMMA and HfO_2 , and a triple-layer gate insulator are compared in this graph

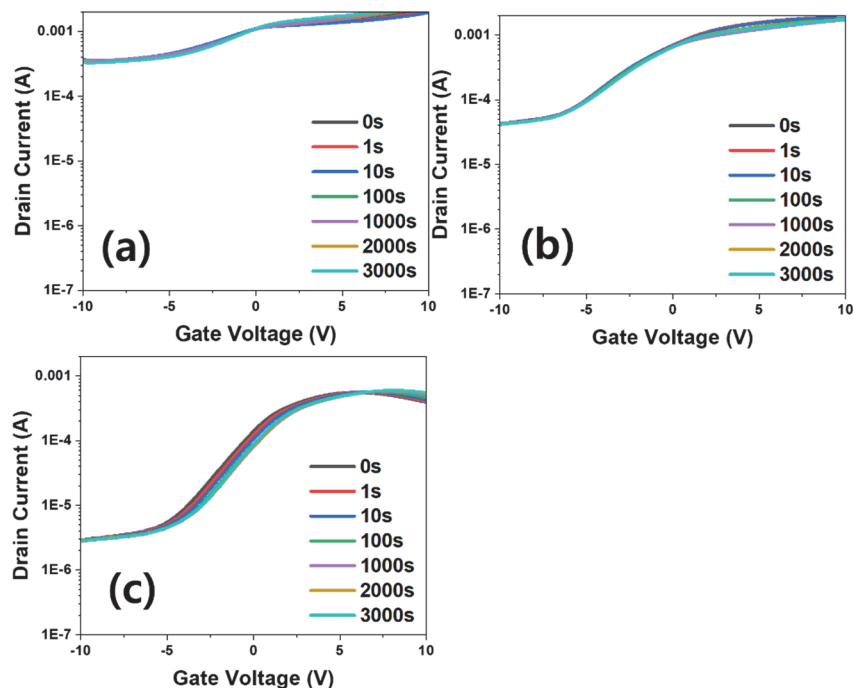


Fig. 5. Transfer characteristics of oxide TFTs using (a) (PvP-co-PMMA)+ HfO_2 , (b) HfO_2 , and (c) HfO_2 +PvP-co-PMMA)+ HfO_2 gate insulators with a positive gate bias applied directly ($V_{GS} = +10 \text{ V}$)

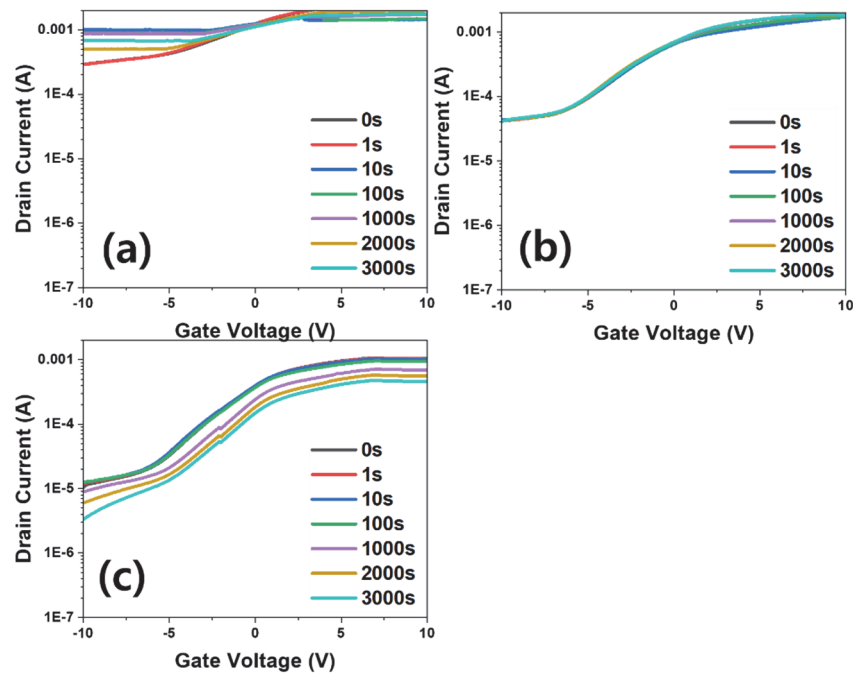


Fig. 6. Transfer characteristics of oxide TFTs using (a) (PvP-co-PMMA)+HfO₂, (b) HfO₂, and (c) HfO₂+PvP-co-PMMA)+HfO₂ gate insulators with a negative gate bias applied directly ($V_{GS} = -10$ V)

4 Conclusion

This study presents a hybrid inorganic–organic–inorganic gate insulator for stretchable oxide TFTs. Key findings include: In first, we stirred at 75°C instead of room temperature improves the cross-linking reaction's homogeneity and yield by reducing the viscosity of the reactants. Additionally, the addition of moisture-absorbing MgSO₄ improves the on-, off-current and subthreshold swing (S.S.) values of the oxide TFT devices by removing impurities from the gate insulator and reducing the roughness of the thin film. Based on this, the electrical characteristics were assessed when a hybrid structure with both organic and inorganic layers was used to create the gate insulator while keeping the stirring conditions at 75°C and adding MgSO₄. Consequently, an inorganic-organic-inorganic triple-layer structure was suggested, which guarantees superior tensile strength in comparison to a single HfO₂ layer and reduces the oxide semiconductor layer degradation brought on by organic materials when utilizing a PvP-co-PMMA and HfO₂ double-layer structure. This study is important because it addresses the leakage current problem that occurs when employing an organic single-layer gate insulator, even though the electrical characteristics are not as good as those of devices using an inorganic single-layer gate

insulator. The gate insulator structure used in this work is a multilayer structure of organic and inorganic insulating films created at comparatively low processing temperatures. In doing so, it creates a stretchable gate insulator that makes it possible for semiconductor devices to have extremely dependable stretchable architectures. Additionally, this approach has the potential to be used in the bio-industry, augmented-, virtual-reality (AR/VR) displays, and future next-generation mobile devices by altering the substrate structure to accommodate the high degree of stretchability required in both vertical and horizontal directions for stretchable displays.

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Conflict of Interest

The author(s) (Sung-Hwan Choi) currently serves on the editorial board of JEEM, but was not involved in any part of the publication process. Other than this, the authors declare that they have no relevant potential conflicts of interest.

Author Contributions

Chae Yeon Kim: Writing - Original Draft, Conceptualization, Validation, Formal analysis.

Sung-Hwan Choi: Writing - Original Draft, Writing - Review & Editing, Visualization, Supervision, Project administration, Funding acquisition.

Data Availability

Data available on request from the authors.

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